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Application Note

ECLinPS™ Circuit Performance at Non-Standard VIH Levels

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This application note explains the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

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Introduction

When interfacing ECLinPS devices to various other technologies times arise where the the input voltages do not meet the specification limits outlined in the ECLinPS data book. The purpose of this document is to explain the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

The results outlined in this document should not be viewed as guarantees by Motorola but rather as representative information from which the reader can base design decisions. It is up to the reader to assess the risks of implementing the non-standard interface and deciding if that level of risk is acceptable for the system design. Motorola's guarantee on V_{IH} will continue to be the specification standards established for the 10H™ and 100K ECL technologies.

Overview

The upper end of the V_{IH} spec of an ECLinPS, or any other ECL, input is limited by saturation affects of the input transistor. Figure 1 below illustrates a typical ECL input (excluding pulldown resistors and ESD structures); the structure is a basic differential amplifier configuration. With a logic HIGH level asserted at the input the collector of that transistor will be pulled down below the V_{CC} rail by the gate current passing through the collector load resistor. The voltage at the collector of the input transistor (V_C) will be dependent on the gate current and the size of the collector load resistor associated with the input gate.

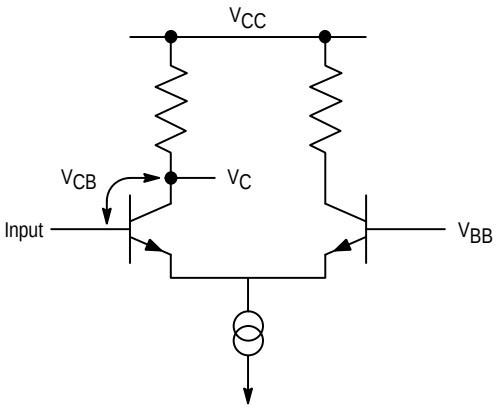

Figure 1. Typical ECLinPS Input Structure

As the input V_{IH} increases towards V_{CC} the collector base junction of the input transistor becomes forward biased; as this forward bias condition increases the transistor will move into the saturation region. The value of V_{CB} at which the transistor begins to saturate is process dependent and will vary from logic family to logic family. Fortunately the MOSAIC III process used to implement the ECLinPS family incorporates a deep n+ collector doping. This deep collector helps to mitigate the effects of saturation of transistors by requiring a larger collector-base forward bias to enter the saturation region.

V_{IH}max and the ECLinPS Family

As previously mentioned the MOSAIC III™ process allows for ECLinPS devices to operate at V_{IH}max levels somewhat higher than those specified in the databook, however the exact value of V_{IH} for which saturation problems will occur varies from device to device and even among different inputs for a given device. This variation is a result of the different input configurations used on the various inputs of ECLinPS devices.

The easiest way to define an acceptable V_{IH}max for each device in the family is to define at what point the input transistor will saturate and specify for each input what the worst case input transistor collector voltage will be. With this information designers will be able to determine on a part by part, input by input basis what input voltage levels will be acceptable for their application.

Simulation Results

The input saturation phenomenon was characterized through SPICE simulations and the results will be reported in the following text. For simplicity of simulation a buffer similar to the E122 was used. Since the outputs of this buffer drive off chip, the V_{IH}max performance of this structure will be worse than the typical input structure. Both a 100K and a 10H style buffer were analyzed to note any discrepancies between the two standards. As expected the simulation results showed no difference in the saturation susceptibility of a 100K versus a 10H style buffer. Therefore the simulation results of only the 100K style buffer will be presented to minimize redundancy of information.

The following text will refer to Figures 4–8 in the appendix of this document. Figures 4–8 are graphical plots of the input and output waveforms of an E122 style buffer (structure similar to that of Figure 1) for various V_{IH} levels. V(in) represents the input voltage while V(q) and V(qb) represent the output voltages. The V(vbb) line was included for measurement purposes only and will be ignored.

Figure 4 represents the "standard" operation of the device as a standard V_{IH} input was used. Note that in this condition the propagation delays measure in the 215–225ps range and the I_{INH} was 42.5µA. The I_{INH} of this device is simply a measure of the base current of the input transistor when that transistor is conducting current. We will be monitoring both of these conditions as well as any degradation in the output waveforms as a sign of the input transistor becoming saturated. As can be seen in Figures 5 and 6 none of the parameters change for V_{IH} levels of up to –0.4V. With a collector voltage, V_C, of –1.0V these V_{IH}'s correspond to a collector base forward bias of 600mV. As the V_{IH} of the input moves closer to V_{CC}, Figures 7 and 8, three phenomena start to occur: the I_{INH} increases, the delays increase and significant changes occur to the output low level of the QB pin.

In Figure 7 the I_{INH} of the input transistor has more than doubled from the "standard" level. This increase in base current leads to an increase in the V_{OL} level as the collector current must reduce to maintain the constant emitter current. As the collector current reduces, the IR drop across the collector load resistor reduces, thus raising the V_{OL} level on the QB output. Although the V_{OL} level has shifted the overall propagation delay has remained essentially unchanged.

Finally, when the input is switched all the way up to V_{CC} the V_{OL} level no longer remains in spec as the input base current has jumped to almost 1ma and there has been significant degradation in the high-low propagation delay. It is apparent that for this condition an E122 style buffer will not perform adequately for most systems.

From this information it can be concluded that for a collector-base forward bias of ≤600mV there will be no adverse conditions on the performance of the device. The performance starts to degrade with further forward bias until at a forward bias voltage of ≈1.0V the device will fail both its DC and AC specifications.

ECLinPS Input Structures

There are four basic input structures which will affect the V_{IH}max performance of ECLinPS devices. The four structures are as follows: an internal buffer, an external buffer, an emitter follower input buffer and a series gated emitter follower input.

The internal buffers are input structures whose outputs drive other gates internal to the device, the voltage swings of the input transistor collectors (V_C) on these devices will be ≈800mV. An external buffer is one in which the outputs are fed external to the chip. Because of the relatively large base drive of the output emitter follower for these structures the V_C voltage will typically be a couple hundred milivolts lower than for the internal buffer. Note that because of the larger output swings of a 10E device, a 10E style external buffer will require a V_{IH}max input level more near the specified value. Both of these structures are similar to that pictured in Figure 1.

The third and fourth structures are somewhat different in design than the first two. Figure 2 illustrates an emitter follower input structure. For the basic emitter follower input the input voltages are dropped by an additional V_{BE} (≈800mV) before they are fed into the differential amplifier input gate. The switching reference is also shifted down by one diode drop to remain centered in the input swing. Obviously this input structure will represent the "best case" in the area of extended V_{IH}max performance. In fact this type of input structure will allow for input voltages even several hundred millivolts above the V_{CC} rail. This characteristic makes these type devices ideal for interfacing with differential oscillators whose outputs lack any DC offset. In the emitter follower structure the limiting factor will be the saturation of the emitter follower device whose collector is at V_{CC}. From the previous simulation results this would suggest a maximum V_{IH} of +0.6V.

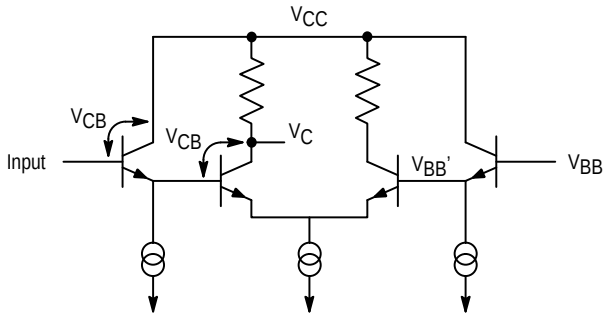

Figure 2. Emitter Follower Input Structure

The series gate emitter follower input will represent the absolute worst case situation for a 100E device. Figure 3 represents a series gate emitter follower input for a 10E and a 100E device. From this figure it is apparent that the lower switching level (B input level) is going to be much more susceptible to V_{IH}max for the 100E device than the 10E device. The two diode drops used for the 10E device is not possible for a 100E device due to the smaller V_{EE} voltage of a 100E device.

To summarize the external gate will represent the worst case V_{IH}max situation for a 10E device while the series gate emitter follower case will represent worst case for a 100E device. In either situation the standard emitter follower will allow the most leeway for non-standard V_{IH}max performance.

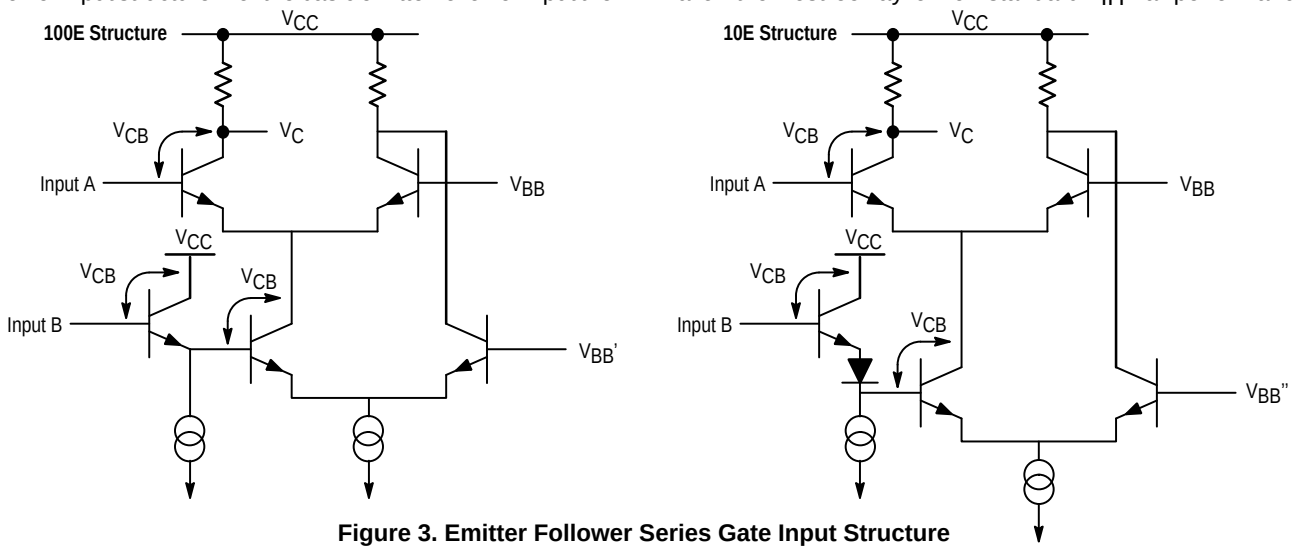

Figure 3. Emitter Follower Series Gate Input Structure

Other Considerations

When driving ECLinPS devices with other than standard input levels there is another phenomena that should be considered; namely effects of non-centered switching references on the AC performance of a device. For non-standard input voltages the midpoint of the voltage swing may not correspond to the internal V_{BB} switching reference. If this is the case the resulting AC variation should be included in the evaluation of a design.

An input voltage swing not centered about the switching reference will exhibit a delay skew between the two input edge transitions. The size of this skew will be dependent on both the voltage offset of the reference voltage and the midpoint of the input swing and the slew rate of the input as it passes through the threshold region. As an example for the case in which the V_{IH} = –0.5V and the V_{IL} remains at –1.7V the midpoint of the swing will be at –1.1V versus a –1.32V V_{BB} reference. With a typical slew rate of 1ps/mV for ECLinPS type edge rates the rising input edge delay will be 220ps longer than normal and the falling edge delay will be 220ps faster. This results in a 440ps skew between the two input transitions that would not be seen for an ideal switching reference.

The only means of correcting this skew is to lower the V_{IL} level to recenter the swing or provide a different switching reference for the device. The latter can be accomplished by buffering the signal with a differential input device with one input tied to an externally generated switching reference. Raising the V_{IL} level is not recommended due to the obvious loss of low end noise margin accompanied by any such shift.

Conclusions

Simulations show that forward bias levels of ≤600mV on the input transistor will keep the input transistor in the active region and the performance of the device will not be compromised. This forward bias voltage can be increased with varying degrees of performance degradation to levels somewhat higher than 600mV. Initial effects will be an increase in the I_{INH} current and a decrease in the output V_{OL} level on the QB output of the input gate. As the forward bias increases further the propagation delays through the device will be adversely affected.

The following example will outline the use of the table in the appendix to analyze the potential performance of a design using non-standard V_{IH} levels. If a design called for the 10E112 and the 10E416 to be driven by a –0.2V input signal a designer would want to know if these two devices would perform to specifications under these conditions. From the table the worst case collector voltage V_C would be –1.05V and 0.0V respectively. Subtracting these values from –0.2V yields forward bias voltages of 850mV and –200mV respectively. From this information the designer would conclude that the 10E416 will function with no problems however the 10E112 could suffer performance degradation under these same conditions.

The device information contained in the appendix of this document will provide designers with all of the information necessary to evaluate the input transistor forward bias conditions for all of the ECLinPS devices for different input voltages. With these numbers and the information provided in this document designers will be able to make informed decisions about their designs to meet the performance desired at an acceptable level of risk.

Appendix

Device	Input	Input Structure	V_C (10E Typical) (V)	V_C (10E Worst Case) (V)	V_C (100E Typical) (V)	V_C (100E Worst Case) (V)
E016	All	INT	–0.80	–0.90	–0.80	–0.90
E101	All	EF	–0.15	–0.25	–0.10	–0.20
E104/107	Dna	EXT	–0.95	–1.05	–0.90	–1.00
	Dnb	SG	–0.50	–0.60	–1.20	–1.30
E111	All	INT	–0.80	–0.90	–0.80	–0.90
E112	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	EN/	INT	–0.80	–0.90	–0.80	–0.90
E116	All	EXT	–0.95	–1.05	–0.90	–1.00
E122	All	EXT	–0.95	–1.05	–0.90	–1.00
E131	D	INT	–0.90	–1.00	–0.90	–1.00
	Other	SG	–0.50	–0.60	–1.20	–1.30
E141	All	INT	–0.80	–0.90	–0.80	–0.90
E142	All	INT	–0.80	–0.90	–0.80	–0.90
E143	All	INT	–0.80	–0.90	–0.80	–0.90
E150	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	Other	INT	–0.80	–0.90	–0.80	–0.90
E151	All	INT	–0.80	–0.90	–0.80	–0.90
E154	All	INT	–0.80	–0.90	–0.80	–0.90
E155	All	INT	–0.80	–0.90	–0.80	–0.90
E156	All	INT	–0.80	–0.90	–0.80	–0.90
E157	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90
E158	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90
E160	R, CLK	SG	–0.50	–0.60	–1.20	–1.30
	Other	INT	–0.80	–0.90	–0.80	–0.90
E163	All	INT	–0.80	–0.90	–0.80	–0.90
E164	All	INT	–0.80	–0.90	–0.80	–0.90
E166	All	INT	–0.80	–0.90	–0.80	–0.90
E167	All	INT	–0.80	–0.90	–0.80	–0.90
E171	All	INT	–0.80	–0.90	–0.80	–0.90
E175	All	INT	–0.80	–0.90	–0.80	–0.90
E195	All	INT	–0.80	–0.90	–0.80	–0.90
E196	All	INT	–0.80	–0.90	–0.80	–0.90
E212	All	INT	–0.80	–0.90	–0.80	–0.90
E241	All	INT	–0.80	–0.90	–0.80	–0.90
E256	All	INT	–0.80	–0.90	–0.80	–0.90
E336	All	INT	–0.80	–0.90	–0.80	–0.90
E337	All	INT	–0.80	–0.90	–0.80	–0.90
E404	All	EF	0.00	0.00	0.00	0.00
E416	All	EF	0.00	0.00	0.00	0.00
E431	All	INT	–0.80	–0.90	–0.80	–0.90
E451	All	INT	–0.80	–0.90	–0.80	–0.90
E452	All	INT	–0.80	–0.90	–0.80	–0.90
E457	Dn	EF	0.00	0.00	0.00	0.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90

INT = Internal Gate; EXT = External Gate; EF = Emitter Follower Input; SG = Series Gated Input

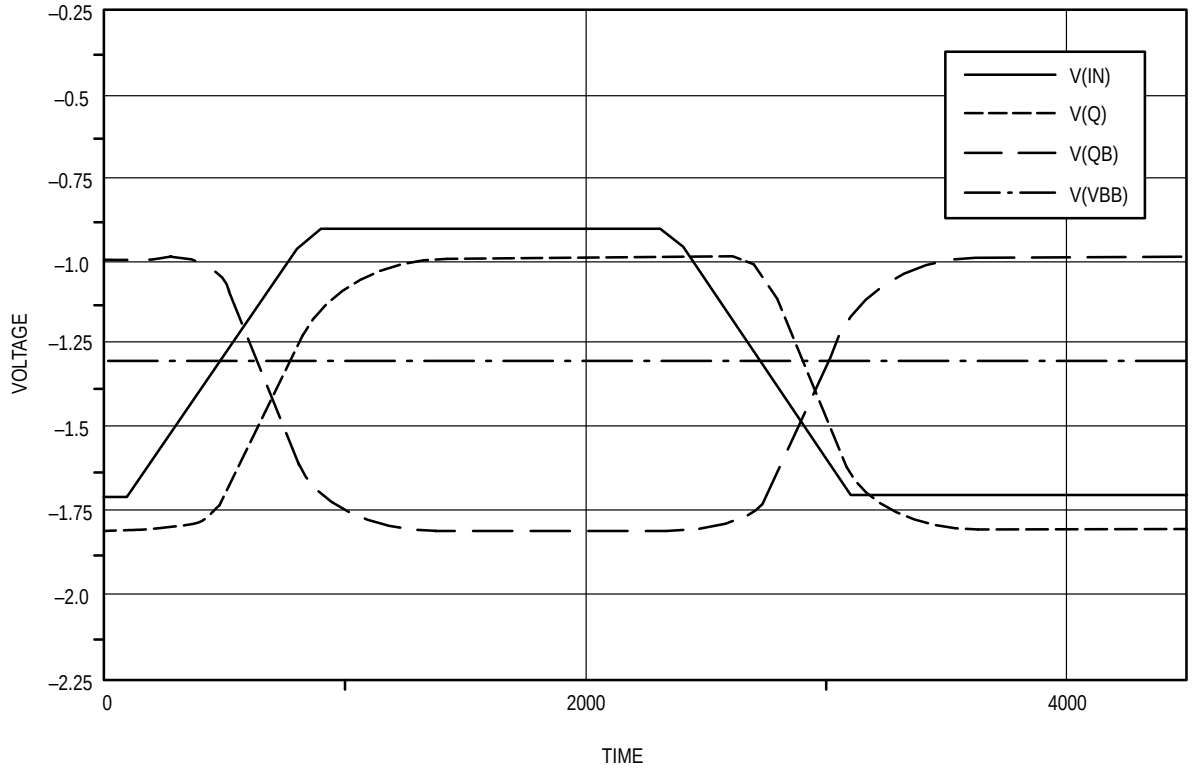

Figure 4. Input and Output Waveforms for V_{IH} = –0.9
(V_{OL} = –1.8; T_{PD}++ = 215ps; T_{PD}– – = 225ps; I_{INH} = 42.5µA)

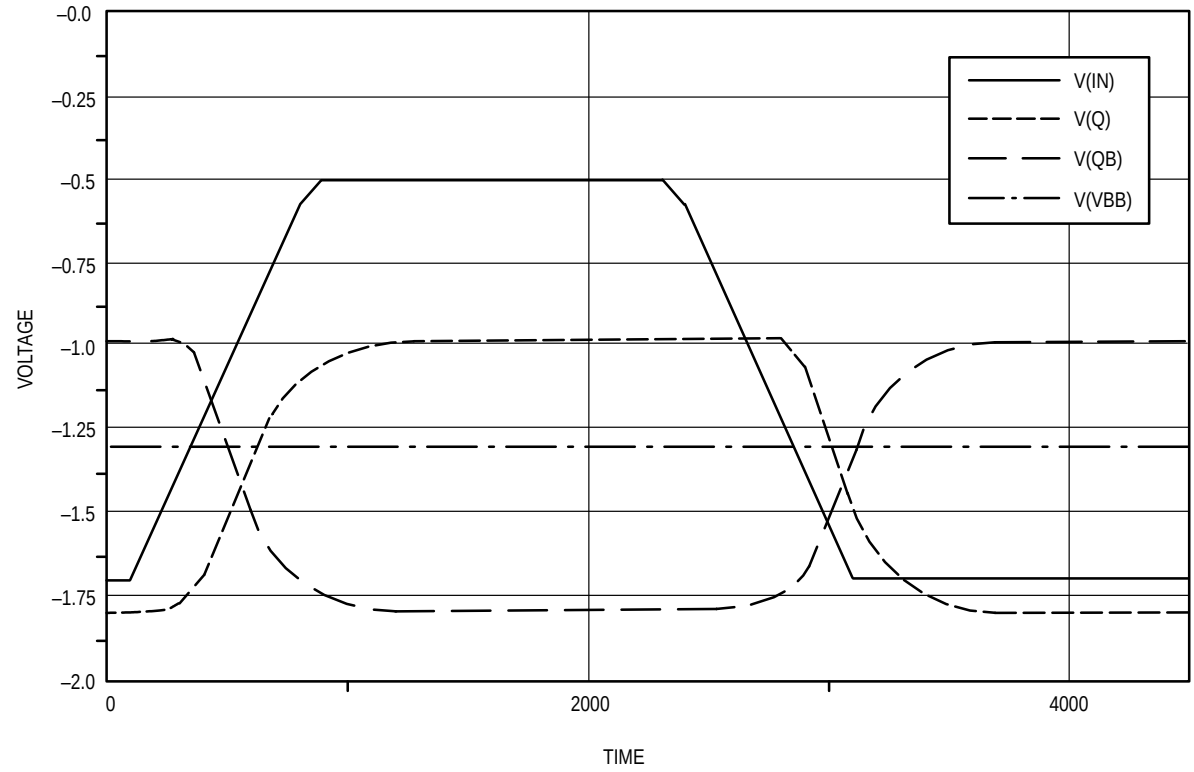

Figure 5. Input and Output Waveforms for V_{IH} = –0.5
(V_{OL} = –1.8; T_{PD}++ = 204ps; T_{PD}– – = 207ps; I_{INH} = 43.4µA)

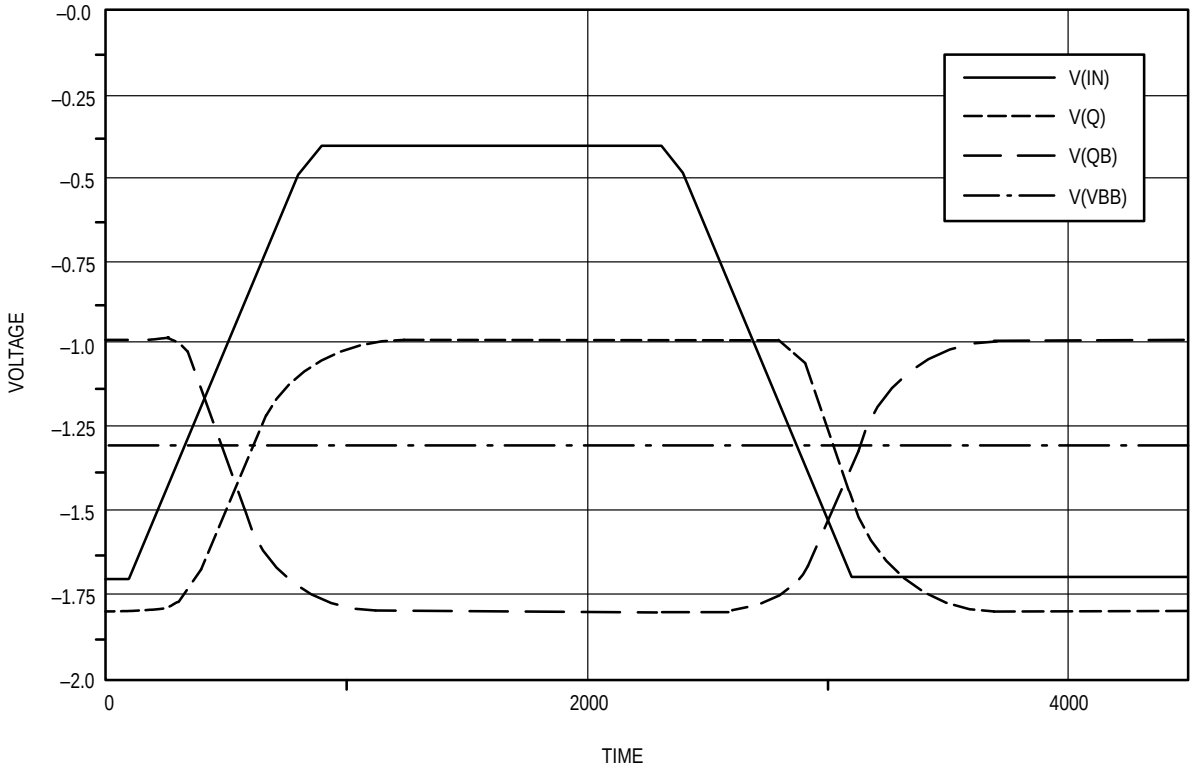

Figure 6. Input and Output Waveforms for V_{IH} = –0.4
(V_{OL} = –1.8; T_{PD}++ = 201ps; T_{PD}– – = 206ps; I_{INH} = 46.7µA)

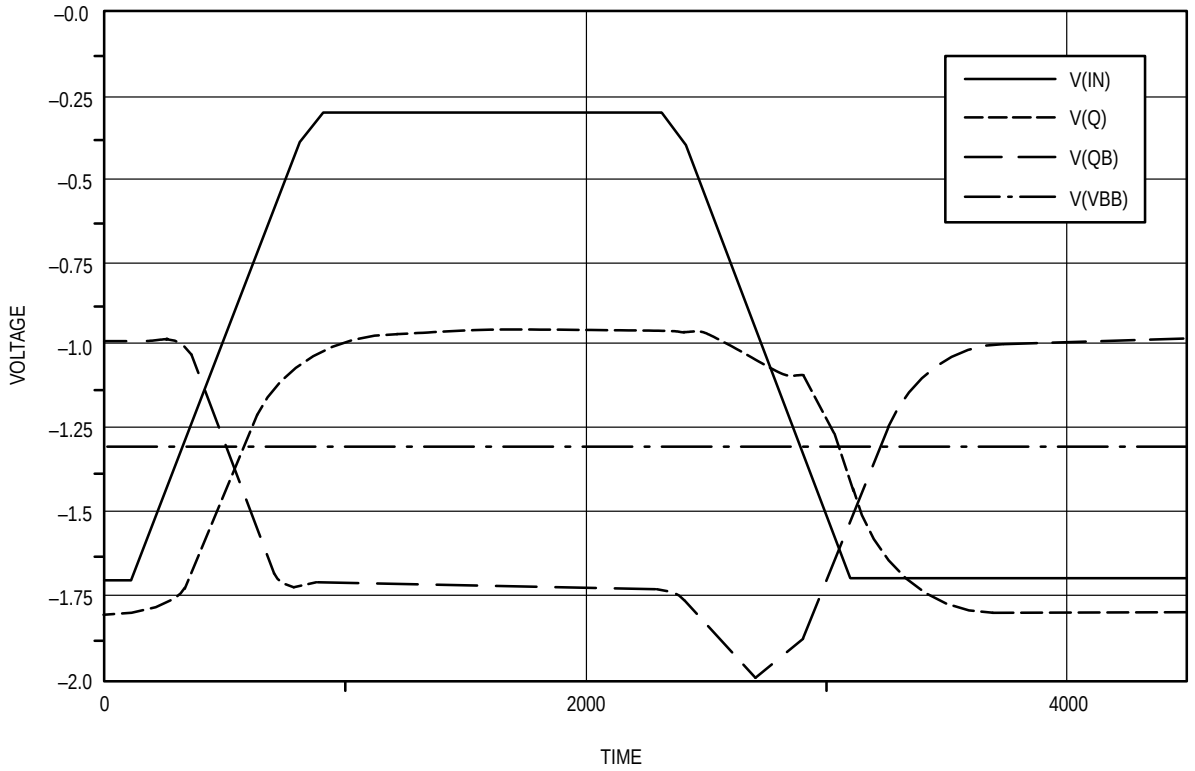

Figure 7. Input and Output Waveforms for V_{IH} = –0.3
(V_{OL} = –1.8; T_{PD}++ = 196ps; T_{PD}– – = 198ps; I_{INH} = 114.8µA)

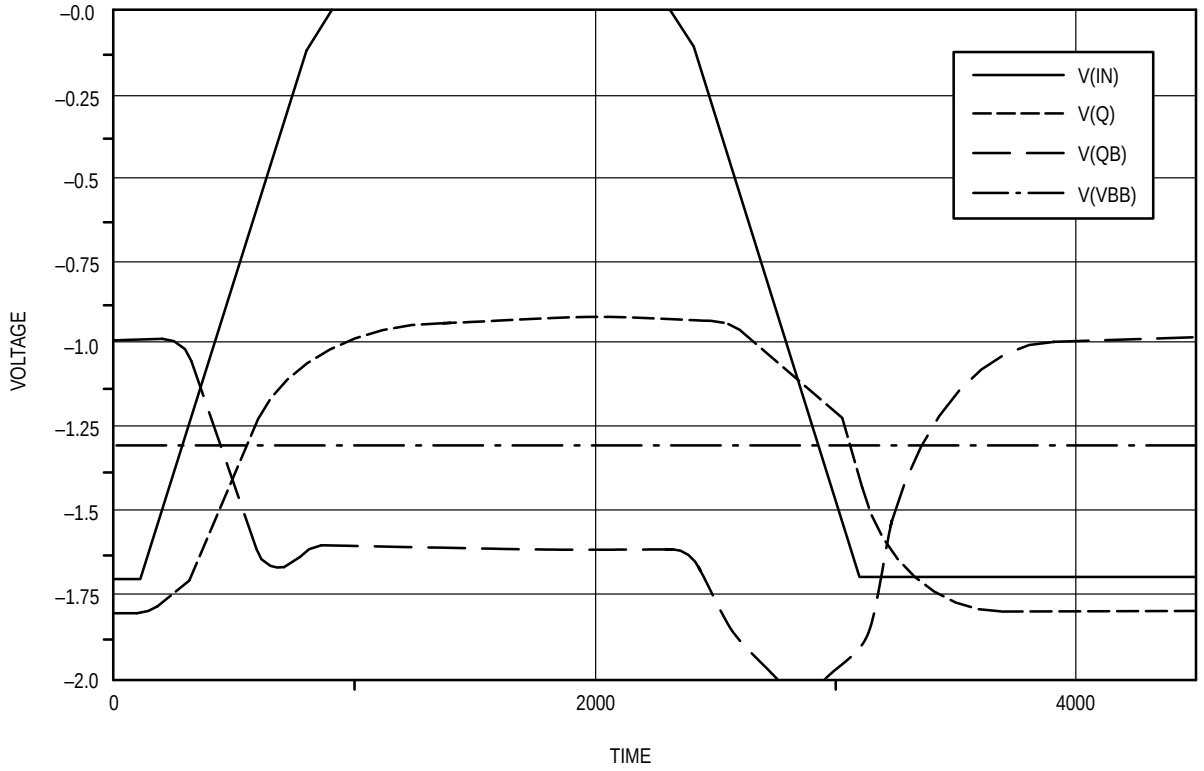

Figure 8. Input and Output Waveforms for V_{IH} = 0.0
(V_{OL} = –1.8; T_{PD}++ = 196ps; T_{PD}– – = 287ps; I_{INH} = 912µA)

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